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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants :	Stephen L. Buchwalter, et al.	**Examiner:**	Khiem D. Nguyen
Serial No.:	09/782,494	**Art Unit:**	2823
Filed:	February 13, 2001	**Docket:**	YOR920000745US1(14029)
For:	BILAYER WAFER-LEVEL UNDERFILL	**Dated:**	December 23, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Sir:

Stephen L. Buchwalter, David Danovitch, Fuad Doany, Claudius Feger, Peter A. Gruber, Nancy C. LaBianca, hereby declare that:

1. We are some of the inventors named in U.S. Patent Application Serial No. 09/782,494 filed February 13, 2001.

2. The remaining joint inventor Revathi Iyenger is no longer affiliated with International Business Machines Corp., the assignee of U.S. Patent Application Serial No. 09/782,494, and despite efforts was unavailable for signature in the present affidavit.

3. We made the invention, which is disclosed and claimed in the present application, in the United States, prior to February 2, 2001, which date is the effective U.S. filing date of U.S. Patent Application Publication Number 2002/0105092 to Coyle ("Coyle").

4. As evidence of the completion of said invention prior to the effective U.S. filing date of Coyle, annexed hereto is Exhibits A(i), A(ii) and B. Exhibit A(i) consists of a true photocopy of the invention disclosure which evidence that the claimed invention was developed in laboratories at IBM Corporation in Yorktown Heights, NY prior to the February 2, 2001 effective U.S. filing date of Coyle. Exhibit A(ii) is a photocopy of "blwluf.prz" the file referenced on Page 3 of the invention disclosure in Exhibit A(i). Exhibit B is a true photocopy of an internal presentation of the subject matter of the present application, which includes a optical micrograph of the conductive bump material and bilayer underfill produced in accordance with the claimed invention. The activity contributing to the development of the claimed invention was conducted under our direct supervision and control prior to the effective U.S. filing date of Coyle. Dates and names have been redacted in the preparation of the photocopies contained in the attached exhibits.

5. The claimed invention is directed to microelectronic packaging, and more particularly to a microelectronic interconnect structure and a method of fabricating the same. The inventive method which utilizes a bilayer polymeric underfill eliminates separate underfill steps that are typically required in prior art methods of fabricating microelectronic interconnect structures.

6. Exhibit A(i) is a photocopy of the original invention disclosure that recognized that a bilayer wafer underfill may be employed to overcome the deficiencies of prior underfill methods, which often result in non-uniform and incomplete underfill that may lead to a shortened fatigue life. Exhibit A(ii) is a photocopy of the attachment referenced on Page 3 of the invention disclosure. Exhibit A(ii) includes figures that illustrate the various steps and elements of the claimed method that correspond to the text included on Pages 2 and 3 of the invention disclosure in Exhibit A(i).

Referring to Exhibit A(ii), FIG. 1(a) illustrates a silicon wafer with ball limiting metallurgy (BLM) that may function as interconnect pads. FIG. 1(b) depicts applying a first underfill layer, i.e., polymeric, on a surface of a semiconductor wafer, as recited in step (a) of Claims 1 and 21. FIG. 1(c) depicts patterning the polymeric material to provide openings in the first underfill layer and exposing the area above the wafer pads, as recited in step (b) of Claims 1 and 21. FIG. 2(a) illustrates applying solder, also referred to as conductive bump material, into the openings, as recited in step (c) of Claims 1 and 21. Turning now to FIG. 2(b), a second polymeric material is deposited atop the first polymeric material and the conductive bump material, as recited in step (d) of Claims 1 and 22. FIG. 3(a) depicts a chip formed by dicing a semiconductor wafer, as recited in step (e) of Claims 1 and 21. FIG. 3(c) depicts bonding at least one of the chips to an external surface, where during bonding the conductive bump material penetrates the second polymeric material and contacts a surface of the external substrate, as recited in step (f) of Claims 1 and 21. As shown, the invention disclosure referenced as Exhibit A(i) discloses the bilayer underfill method of the present invention.

7. Exhibit B provides further evidence of reduction to practice of the present invention prior to February 2, 2001, which date is the effective U.S. filing date of U.S. Patent Application Publication Number 2002/0105092 to Coyle ("Coyle"). Exhibit B is a photocopy of an internal presentation of the subject matter of the application at issue that was given prior to the effective date of the Coyle reference. Included on Page 18 of the presentation in Exhibit B is an optical micrograph of the conductive bump material deposited within the openings of a first polymeric material, where during bonding to an external surface (substrate) the conductive bump material penetrates a second polymeric material and contacts the surface of the external substrate. Still referring to Exhibit B, an optical micrograph of the conductive bump material in conjunction with a B-staged polyimide adhesive (second polymer material) is also included on Page 14 of the presentation.

8. We further declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: 1/14/2004

Stephen L. Buchwalter

Dated: _____

David Danovitch

Dated: 1/15/2004

Fuad Doany

Dated: 1/14/2004

Claudius Feger

Dated: 1/14/2004

Peter A. Gruber

Dated: 1/15/2004

Nancy C. LaBianca

8. We further declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: 1/14/2004

Stephen L. Buchwalter

Dated: 1/16/2004

David Danovitch

Dated: 1/15/2004

Fuad Doany

Dated: 1/14/2004

Claudius Feger

Dated: 1/14/2004

Peter A. Gruber

Dated: 1/15/2004

Nancy C. LaBianca

Gov't Contract

Created By: **Created On:**
Last Modified By: 1 **Last Modified On:**

*** IBM Confidential ***

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

Summary

Status	Under Evaluation
Processing Location	YOR
Functional Area	700 Isaac-Systems, Technology & Science
Attorney/Patent Professional	
IDT Team	
Submitted Date	
Owning Division Select	RES
PVT Score Select	35
Lab	
Technology Code	

Inventors with Lotus Notes IDs

Inventors:

Inventor Name > denotes primary contact	Inventor Serial	Div/Dept	Manager Serial	Manager Name

Inventors without Lotus Notes IDs

IDT Selection

Main Idea

***Title of disclosure (in English)**

Bi-Layer Wafer Level Underfill

***Idea of disclosure**

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of

using the invention.
Flip chip technology has grown quickly in recent years as a means of decreasing the chip footprint while simultaneously increasing the number of possible I/O's. This is because it takes advantage of the chip area for I/O's instead of just the chip periphery as does wire-bonding. Various methods exist for solder bumping wafers, such as evaporation, plating, solder paste screening and more recently, injection molding solder or IMS.

Regardless of how wafers are bumped, typically they are thereafter diced into chips. For DCA or direct chip attach, these silicon chips are bonded directly to a laminate substrate. Since there is significant mismatch of CTE (coefficient of thermal expansion) between silicon and laminate materials, these chips are thereafter underfilled. This greatly increases the fatigue life of the solder bumps. However, underfilling is associated with several manufacturing problems.

- First, the process is somewhat slow. This is due to the typical dispensing method of applying the liquid underfill along at least 2 sides of the chip and letting capillary action pull the liquid completely under the chip.
- Secondly, incomplete underfills may occur. Since it is difficult to determine underfill uniformity, this could lead to excess mechanical stresses on affected bumps. This in turn leads to shortened fatigue life for the affected chip.
- Thirdly, underfilling is yet another packaging process step. Ideally, this step would be eliminated to accelerate the path from wafer to packaged chip.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?
This invention describes a process and structure that addresses all three problems mentioned previously. In effect, a bi-layer wafer level underfill completely eliminates the separate underfilling process as practiced now. Thus, a time-consuming and somewhat problematic manufacturing step is removed. The following description with the aid of the figures serves to outline the key concepts of this invention.

As seen in Fig. 1a, a silicon wafer is at the point where solder bumps are required to prepare it for a flip-chip application. This wafer contains the appropriate BLM Ball Limiting Metallurgy covering the pads which will receive the solder. Fig. 1b shows the application of a patternable dielectric to the wafer front side containing the pads. This material may be applied by a spin coating or similar process. Unlike typical passivation layers though, this material is applied to a thickness roughly ranging between 25 and 75 microns, thicker than usual. The reason for this is its additional function as described shortly. Fig. 1c shows the dielectric layer after the patterning step. The patterning may be done by laser ablation, reactive ion or wet etching. It opens up the areas above the wafer pads.

Fig. 2a shows the key additional functionality of the thicker dielectric layer, namely as a solder mask. Solder is applied into the cavities formed after the dielectric is patterned. The method for this application is IMS Injection Molded Solder, which scans a head containing molten solder over the wafer and fills the cavities. Thereafter the wafer is cooled and the solder solidifies. In effect, this solder mask also serves as the major portion of the underfill as will be seen in the figure 3 descriptions. As seen in Fig. 2b, after the solder is applied, a very thin layer combining flux and adhesive is applied uniformly over the wafer. This again may be done with a spin coating or similar process. Once this layer has hardened, te wafer is ready to be diced into individual IC Integrated Circuit chips.

Fig. 3a shows such a diced chip containing in effect everything required to bond and underfill it to the laminate substrate. Fig. 3b shows the flipped chip being aligned and placed on the laminate substrate. Thus, the solder filled cavities align to the solder receiving pads on the substrate. The chip adheres to the laminate substrate by the step shown in Fig. 3c. Here the assembly is heated to the solder reflow temperature which serves two purposes. One, it activates the fluxing agent in the thin secondary layer thus allowing the solder to penetrate throgh it and wet (metallurgically bond) to the metallized pad on the laminate substrate. Two, it activates the adhesive in this same layer which mechanically bonds the chip to the same substrate. Since this secondary layer is very thin (typically below 12 microns) compared to the

primary layer which serves as the solder mask, there is very little solder volume needed to penetrate through it. Also, during this heating step, this layer thins still further as it bonds to the substrate. Thus most of the solder volume stays within the cavities and is surrounded by the walls of each cavity as is the case with underfill materials.

Thus, we have described a process and structure which eliminates the separate underfilling step. The details of each process step in this invention as outlined above should not be regarded as limiting, but merely as examples. To those skilled in the art, other methods may also be used to accomplish these steps without changing the novel aspects of this invention.


blwlul.PRZ

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?
No flow underfills have more recently become popular. While they eliminate the capillary dispensing time, these must still be applied to te laminate substrate in a separate manufacturing step.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.
Not implemented yet.

***Critical Questions (Questions 1 - 7 must be answered)**

***Question 1** On what date was the invention workable? **lease format the date as MM/DD/YYYY** (Workable means i.e. when you know that your design will solve the problem)

***Question 2** Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?	● Yes ○ No
If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: None yet, but we would present it at a NIST quarterly review possibly o Date Published or Issued:	
Are you aware of any publications, products or patents that relate to this invention?	○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	

***Question 3** Has the subject matter of the invention or a product incorporating the invention been sold, used internally in manufacturing, announced for sale, or included in a proposal?	○ Yes ● No
Is a sale, use in manufacturing, product announcement, or proposal planned?	○ Yes ● No
If Yes, identify the product if known and indicate the date or planned date of sale, announcements or proposal and to whom the sale, announcement or proposal has been or will be made. Product: Version/Release: Code Name: Date: To Whom: If more than one, use cut and paste and append as necessary in the field provided.	

Question 5	
Have you ever discussed your invention with others not employed at IBM?	○ Yes ● No
If yes, identify individuals and date discussed. Fill in the text area with the following information, the names of the individuals, the employer, date discussed, under CDA, and CDA #.	

Question 7	
Was the invention made in the course of any alliance, joint development or other contract activities?	○ Yes ● No ○ Not Sure
If Yes, enter the following :Name of Alliance, Contractor or Joint Developer	
Contract ID number	
Relationship contact name	
Relationship contact E-mail	
Relationship contact phone	

Question 9

What type of companies do you expect to compete with inventions of this type? *Check all that apply*

- ☒ Manufacturers of enterprise servers
- ☒ Manufacturers of entry servers
- ☒ Manufacturers of workstations
- ☒ Manufacturers of PC's
- ☒ Non-computer manufacturers
- ☐ Developers of operating systems
- ☐ Developers of networking software
- ☐ Developers of application software
- ☐ Integrated solution providers
- ☐ Service providers
- ☐ Other (Please specify below)

Patent Value Tool (Optional - this may be used by the inventor and attorney to assist with the evalu

(The Patent Value tool can be used by you or the evaluation team to determine the potential licensing

value of your invention.)

These are the answers which were entered into the **Patent Value Tool.**

Market

What is the anticipated annual market size (in dollars) that will be captured by your invention?
$1B to $5B

Question 1 - How new is the technical field?
Emerging
Question 2 - How central is the invention to the product(s) which might be expected to contain the invention?
Essential
Question 3 - What is the scope of the claim?
Moderate

PORTFOLIO NEED View PPM Needs List
What are the portfolio needs in the area of your invention?
Listed in PPM Needs

EXPLOITATION & ENFORCEMENT
Question 1 - How easily can the use of the invention by a competitor be detected?
With work
Question 2 - How easily can the use of the invention be avoided by a competitor?
With work

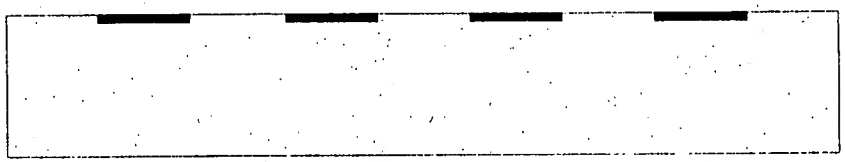
BUSINESS VALUE
Question 1 - What percentage of the companies producing products in the field of this invention might use this invention?
Broadly cloned
Question 2 - What is the value of this patent to current or anticipated Alliance Activity between IBM and other companies?
Some value
Question 3 - What is the value of this patent to current or anticipated Technology Transfer Activity between IBM and other companies?
Some value
Question 4 - Does it result in prestige to IBM?
External

Post Disclosure Text & Drawings
Enter any additional information relating to this disclosure below:

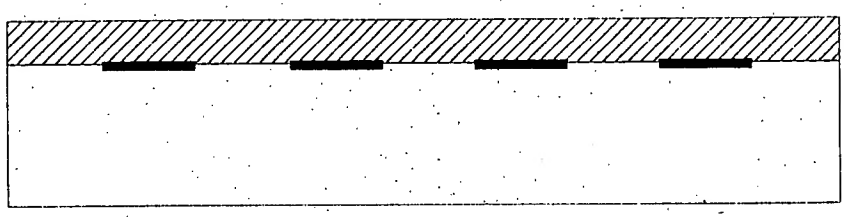
Bi-Layer Wafer Level Underfill

Fig 1

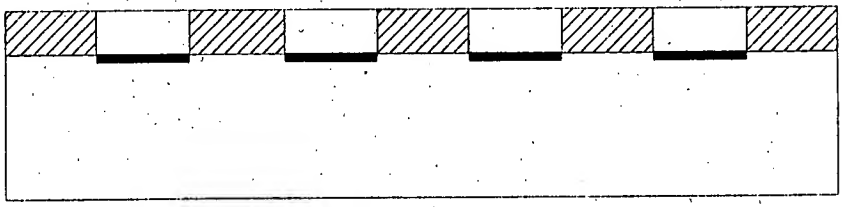
a) silicon wafer with BLM



b) apply first underfill layer



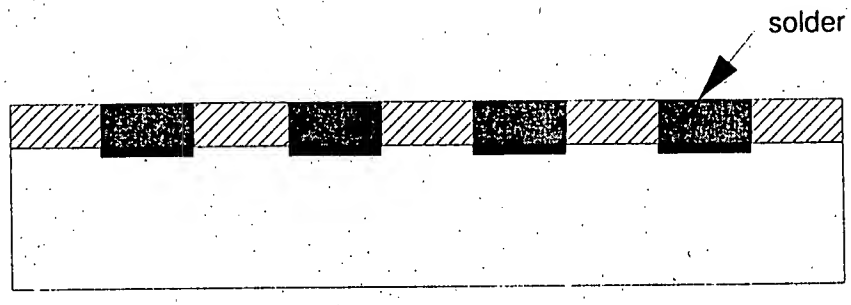
c) pattern first layer



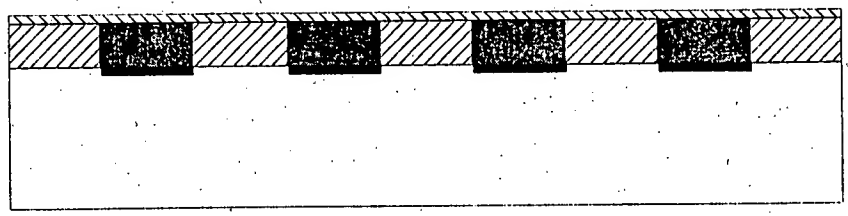
Bi-Layer Wafer Level Underfill

Fig 2

a) apply solder in cavities

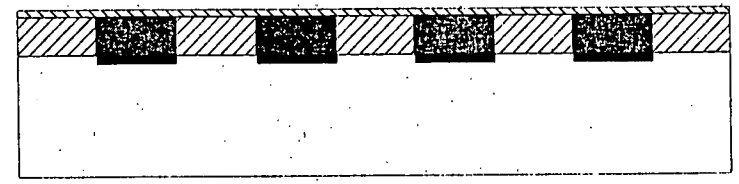


b) apply thin flux-adhesive layer

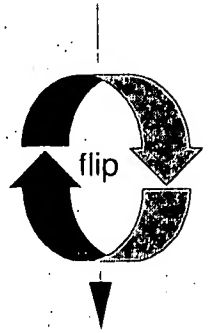


Bi-Layer Wafer Level Underfill

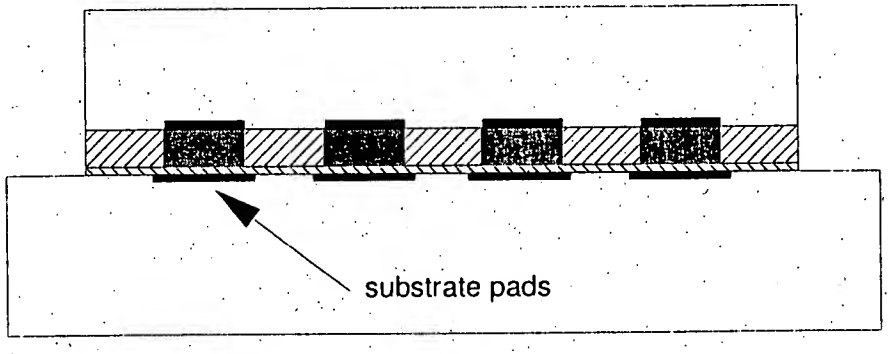
Fig 3



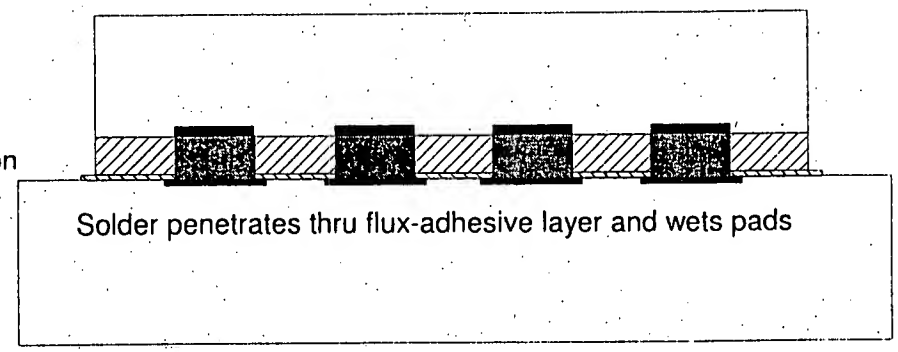
a) Diced chip with bi-layer wafer level underfill before join



b) Flip, align to substrate pads & join



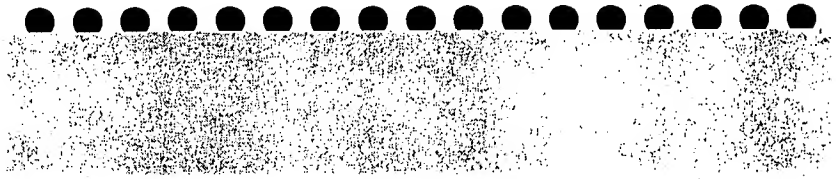
c) solder reflow and flux-adhesive activation



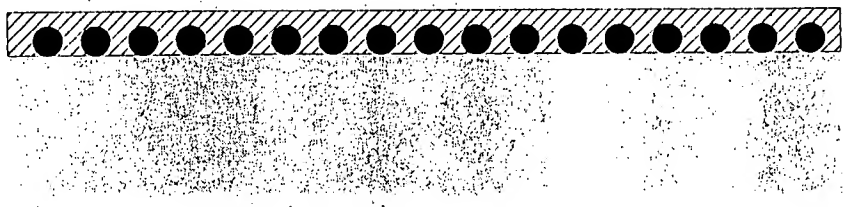
Bi-Layer Wafer Level Underfill

Fig 4

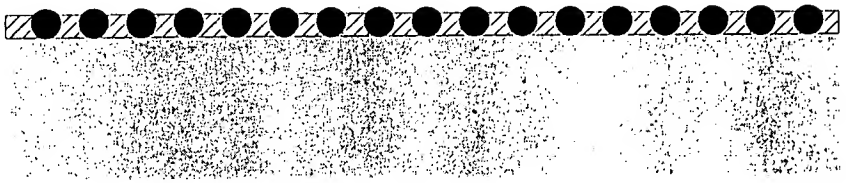
a) bumped silicon wafer



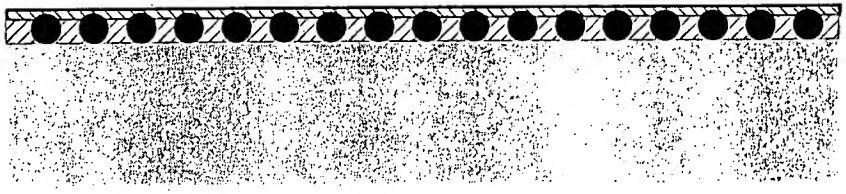
b) apply first underfill layer



c) polish or etch first underfill layer

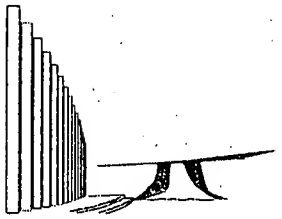


d) apply thin flux-adhesive layer



Wafer Level Underfill Project

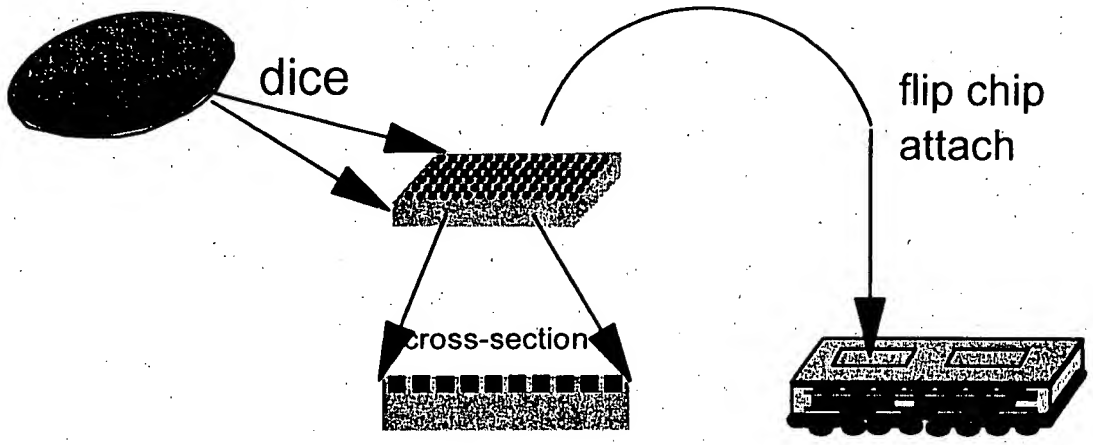
IBM Research
National Starch and Chemical Corp.
NIST-ATP



IBM

T.J. Watson Research Center

Wafer-level Underfill



- Concept: applying interconnect and underfill at wafer level
- Reduce chip assembly to one step
- Eliminate two manufacturing bottlenecks:
  - underfill flow
  - underfill post-cure
- Lead-free
- Reworkable

IBM

Industry Trends and Assumptions

- Strong growth in flip chip market
- Strong semiconductor growth
- Lowest cost solution consistent with electrical performance and form factor requirements will be rewarded in marketplace
- Lead-free interconnects will be required
- Low cost packaging solutions will increase marketshare for IBM semiconductors
- BAT is a major part of packaging cost

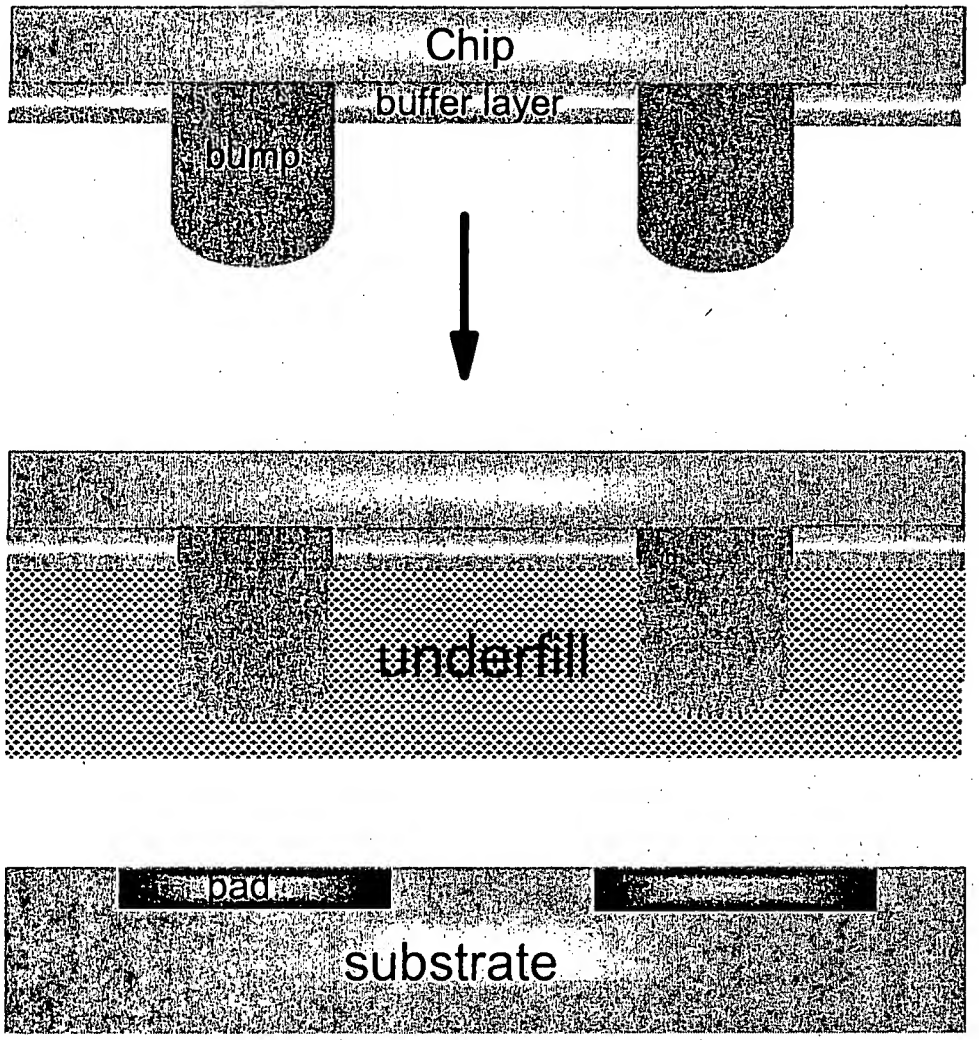
IBM

Wafer-level Underfill - IBM Milestones

- Develop WLUF process schemes;
- Select underfill deposition process on bumped wafers with uniform coating of correct thickness;
- Select approach that has highest likelihood of success, is cheapest, and easiest to integrate in current process flow;
- Ensure compatibility of wafer-level underfill material and process with Pb-free wafer bumping processes;
- Evaluate feasibility of potential reworkable underfill materials;
- Adapt, as necessary, existing wafer dicing process parameters and correlate them to dicing-induced underfill defects.

IBM

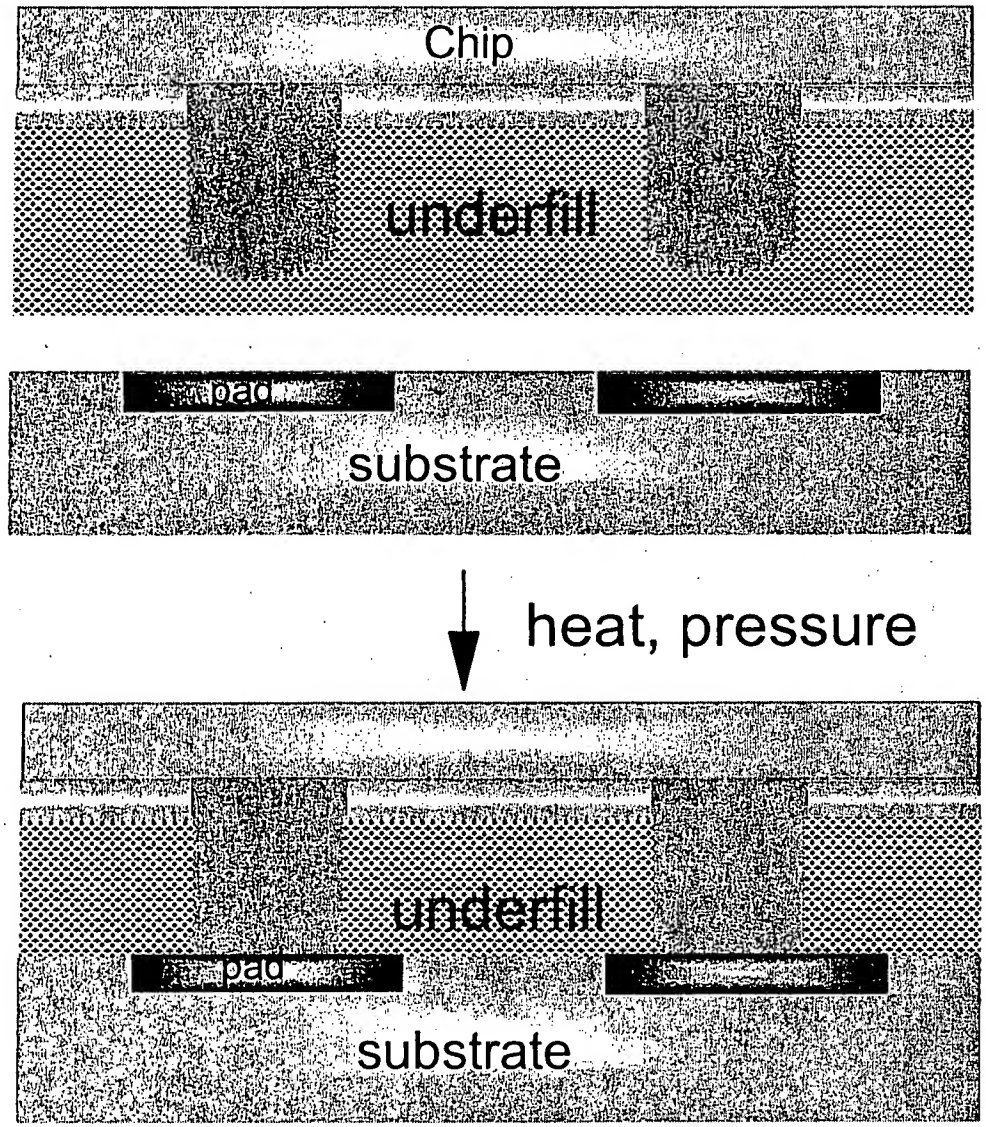
WLUF Project: Bumps First



WLUF apply processes:

- spin coating
- screening
- curtain coating
- etc.

WLUF Project Bumps First



Hierarchy for joining:

underfill softens

then

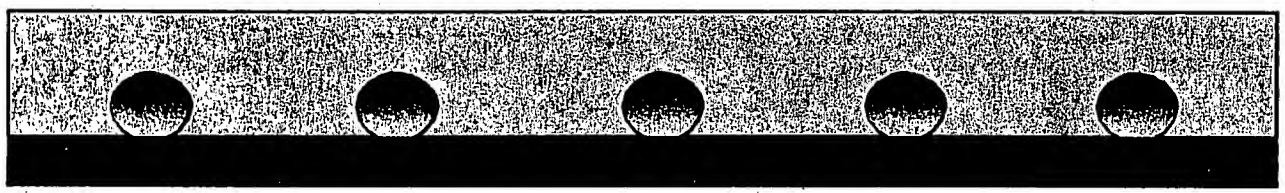
bump softens

Wafer-level Underfill - IBM Milestones

- Develop WLUF process schemes;
- Select underfill deposition process on bumped wafers with uniform coating of correct thickness;
- Select approach that has highest likelihood of success, is cheapest, and easiest to integrate in current process flow;
- Ensure compatibility of wafer-level underfill material and process with Pb-free wafer bumping processes;
- Evaluate feasibility of potential reworkable underfill materials;
- Adapt, as necessary, existing wafer dicing process parameters and correlate them to dicing-induced underfill defects.

IBM

Film Thicknesses



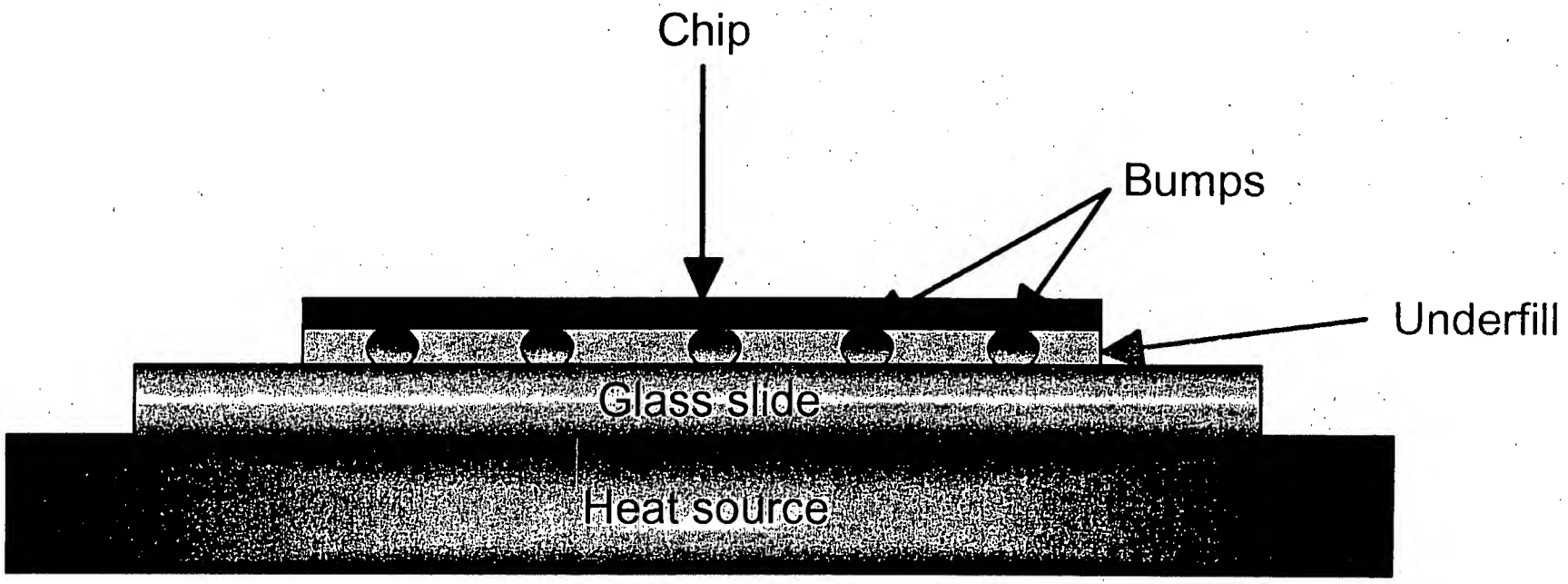
Too much

Too little

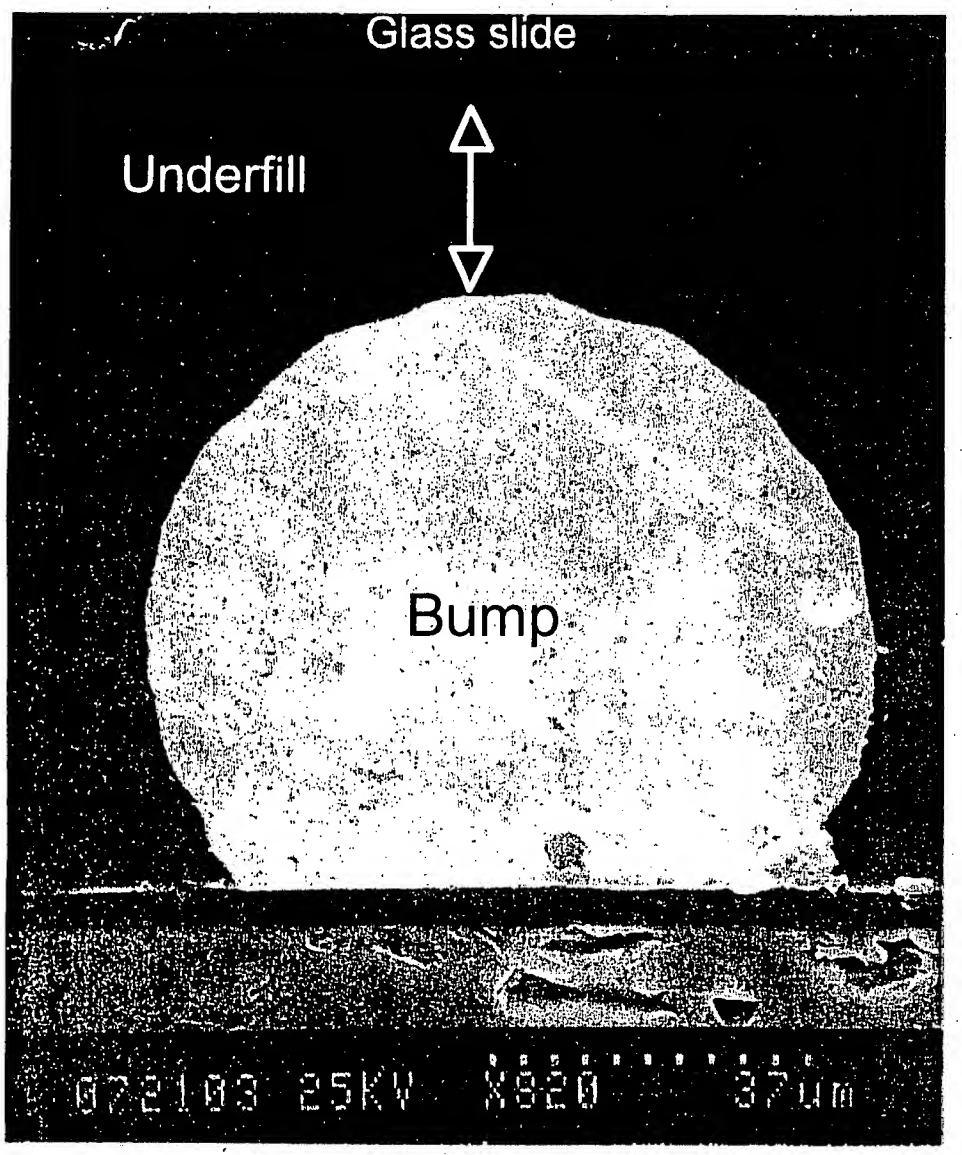
Just right

IBM

Test Structure

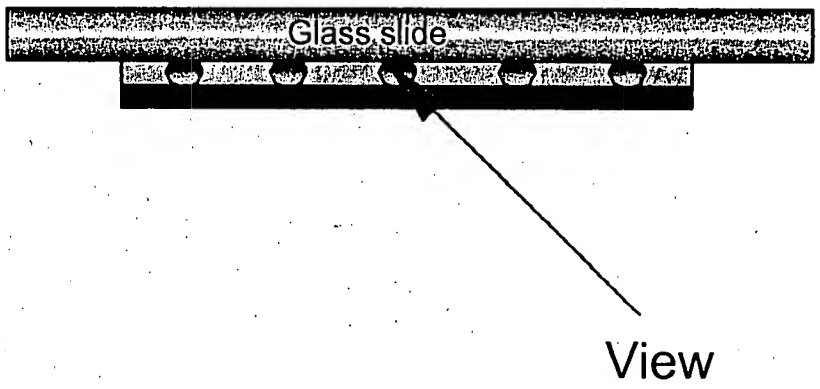


IBM

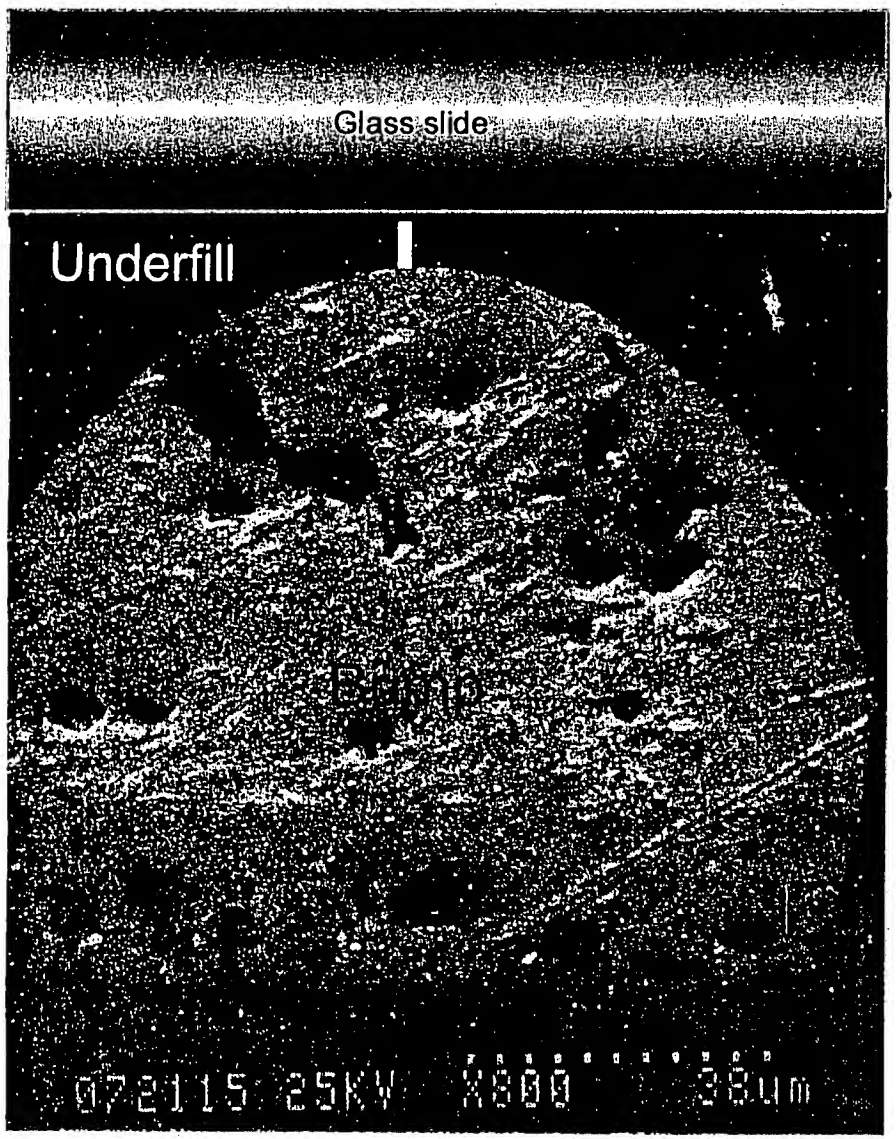


National Starch 19A
220 C Hot Plate
3 minutes Dwell time

No Pressure

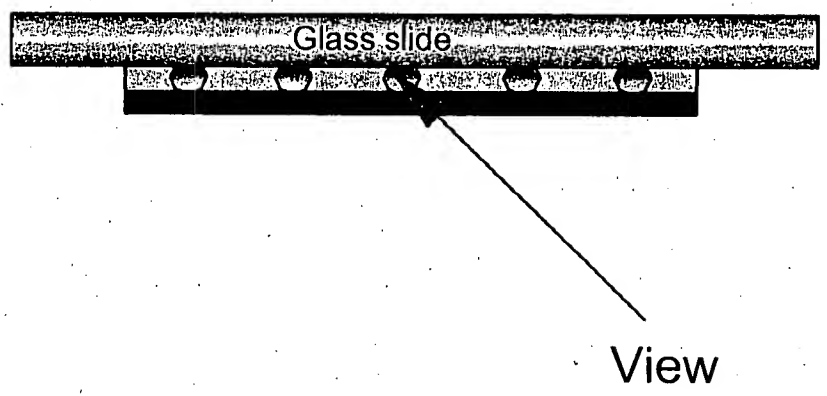


IBM



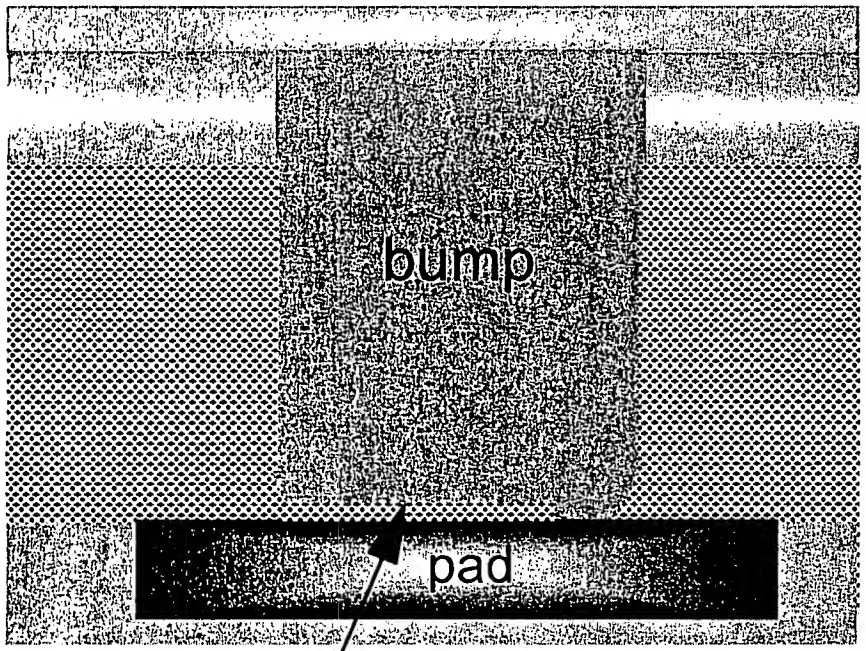
National Starch 19A
200 °C 3 minutes

With Pressure

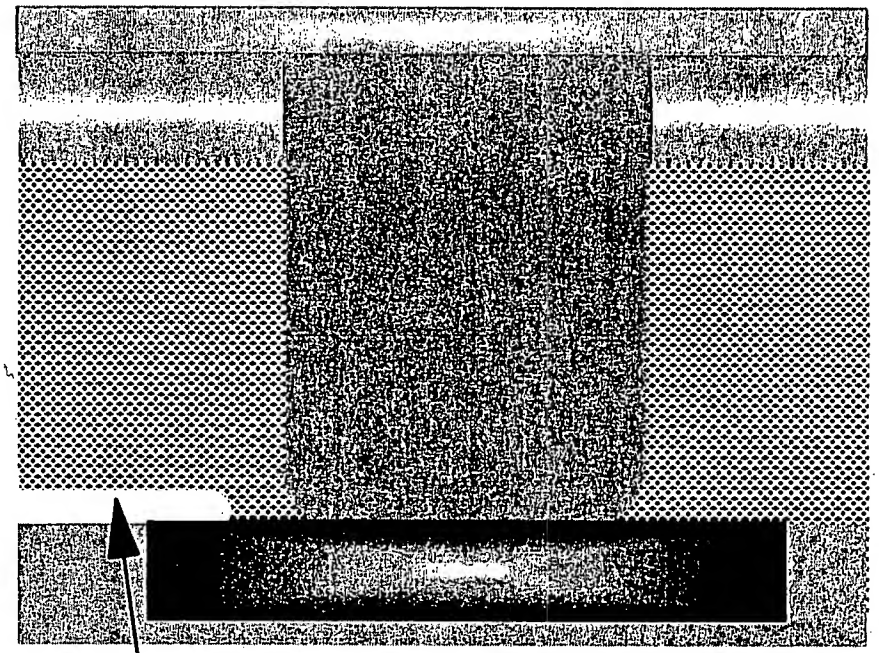


IBM

WLUF Project Bumps First Issues



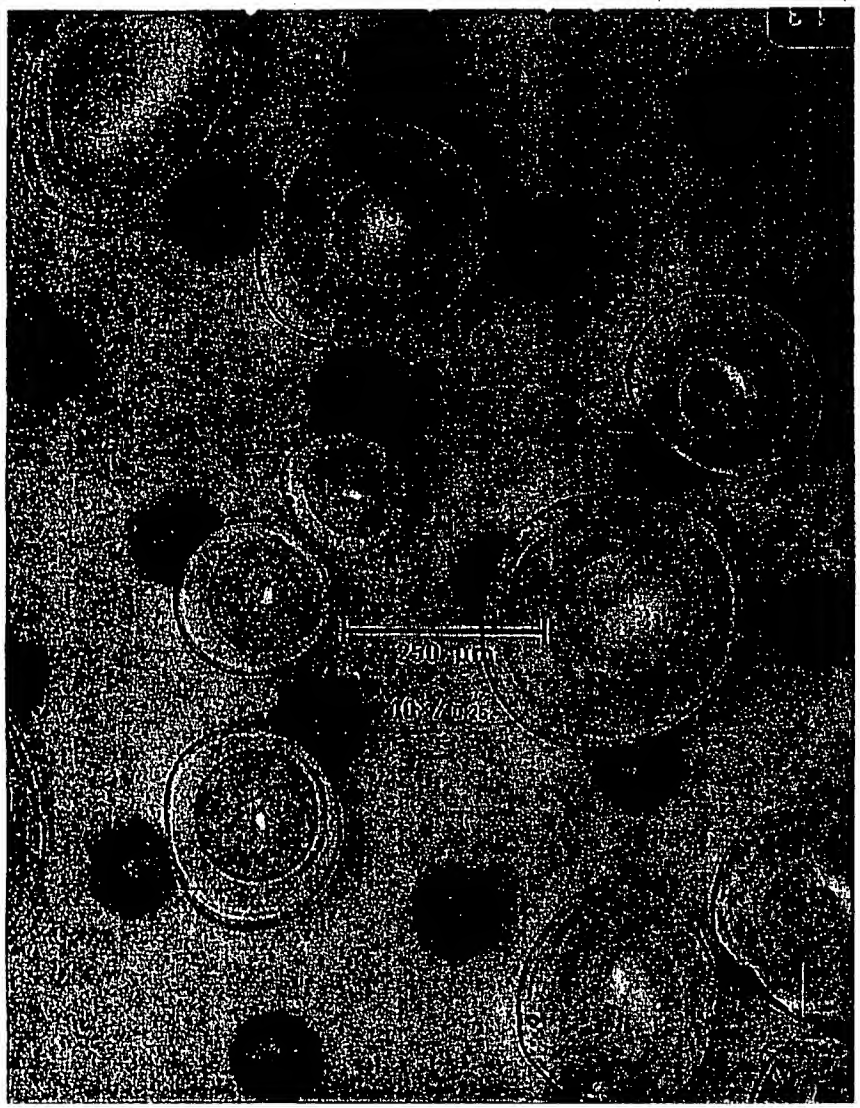
incomplete bump/pad contact



trapped air

fillet formation

Cure/Bond Study - Polyimide Adhesive



B-staged at 90C and 120C

Bonded to glass at 220C using pressure

Major voids / bubbles

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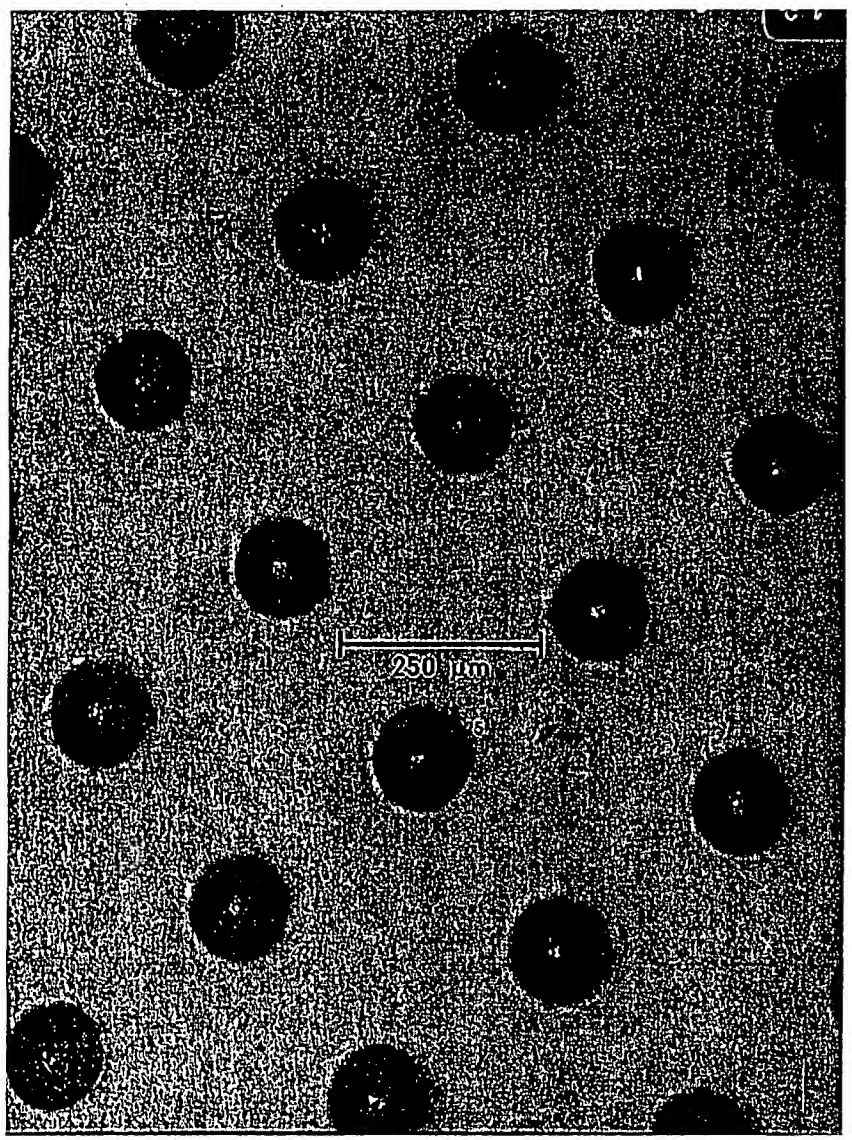
Cure/Bond Study - Polyimide Adhesive



B-staged at 90C, 100C and 120C

Bonded to glass at 220C using pressure

No voids, good wetting of underfill

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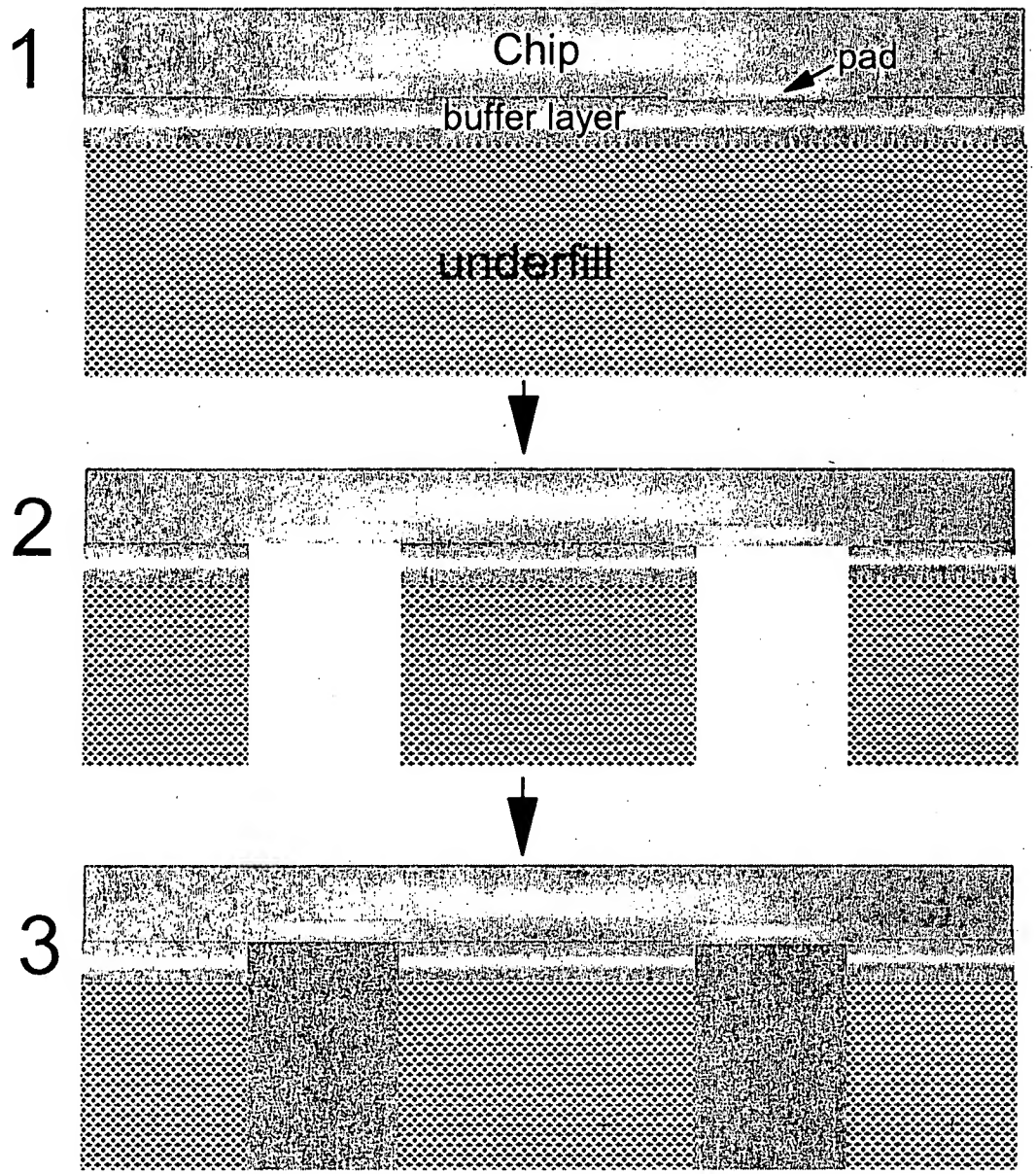
WLUF Project Bumps Second Conductive Adhesive



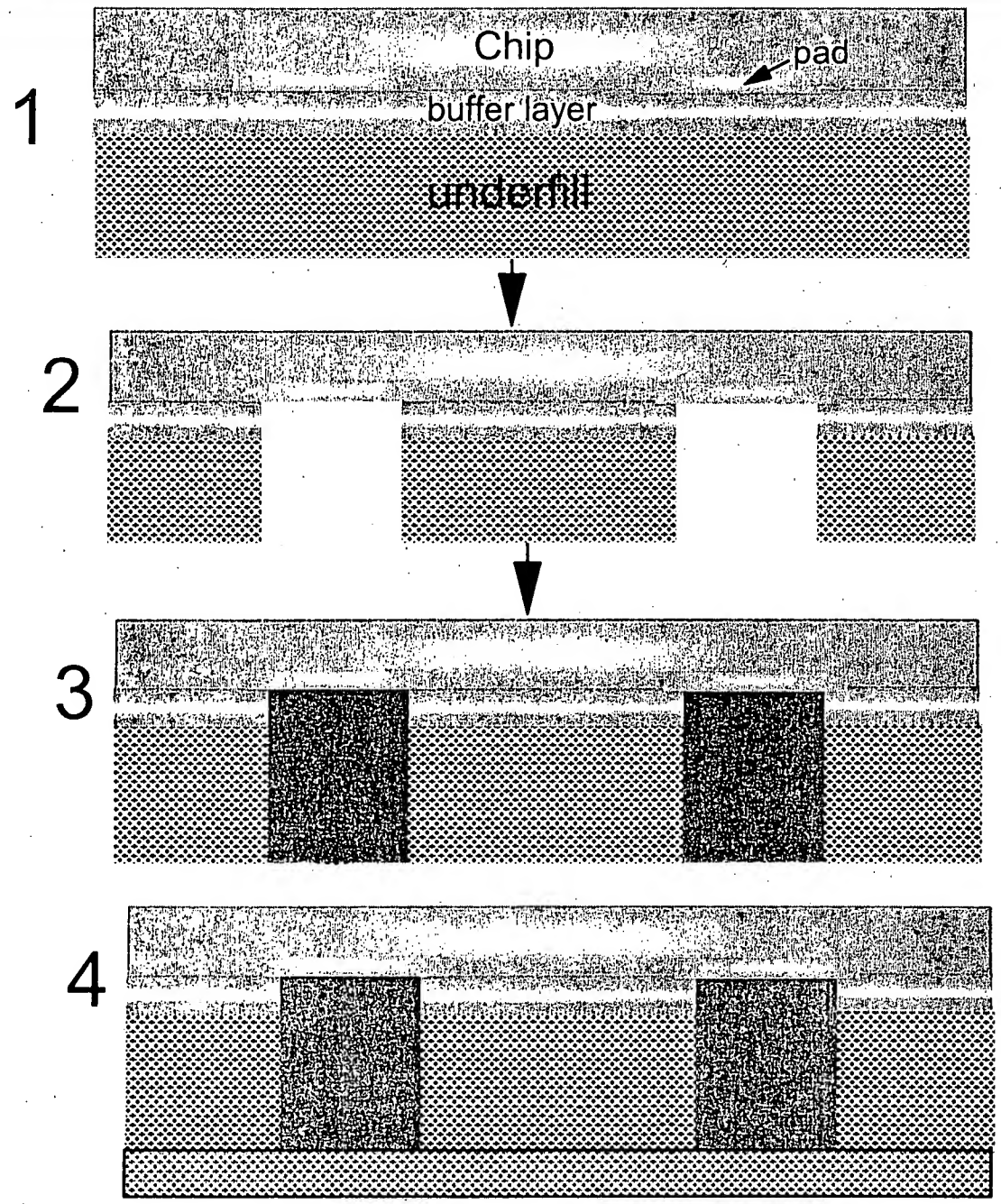
WLUF patterning processes:

- laser ablation
- RIE etching
- wet etching
- photodefinable underfill

Bump fill with conductive adhesive

Join with underfill softening before conductive adhesive

WLUF Project Bumps Second Bi-layer/Solder



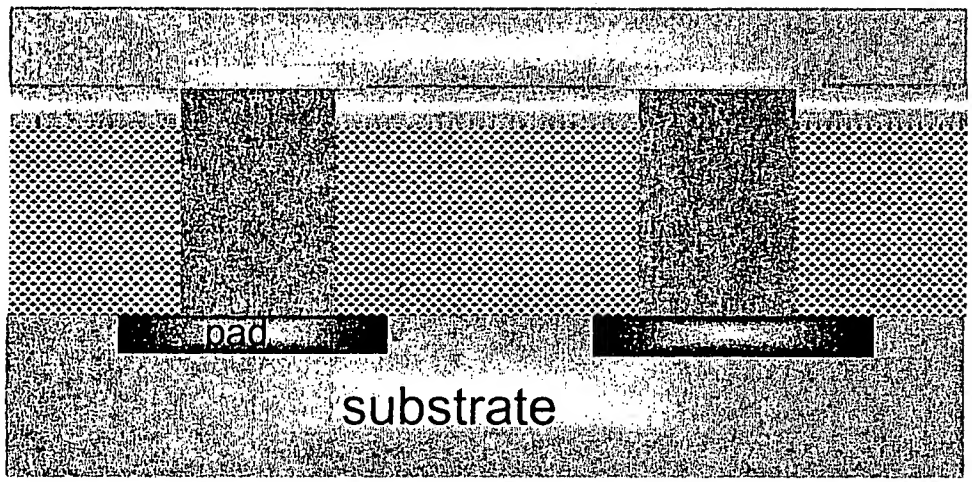
WLUF patterning

Bump fill with molten solder (IMS)

Apply fluxing adhesive

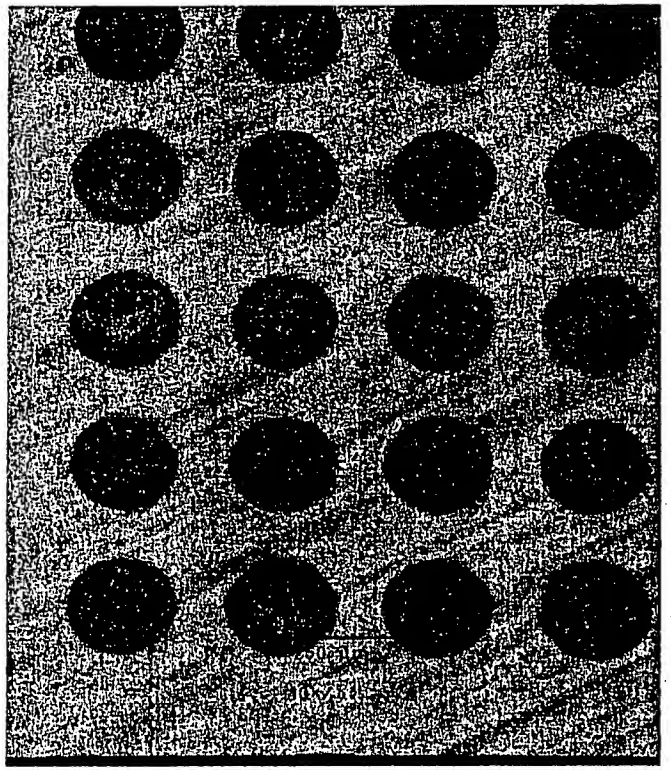
Join through soft, b-staged adhesive

WLUF Project Bumps Second



issues are essentially same as for bump first

Bumps Second - Hole Fill and Bonding



Patterned polyimide adhesive

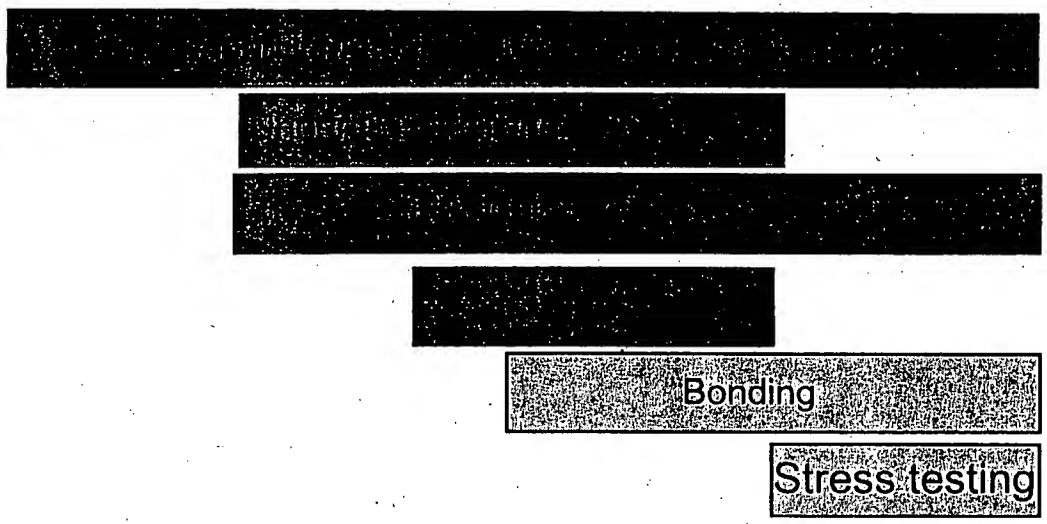
Conductive paste in vias

Bonded to glass at 220C (w/pressure)

Good adhesion to glass

Conductive paste flush with glass

Development Schedule



- ► demonstrate feasibility on test vehicles
- ► workable flip chip attach and reliable flip chip interconnects

- NIST-ATP Support jointly with National Starch:
  - ► 3 Research H/C + post-doc
  - ► National Starch & Chemical team
  - ► Georgia Tech

Two fundamentally different approaches:

- Bumps first: more packaging oriented (receive bumped wafers)
- Bumps second: more wafer fab oriented (change bumping process flow)

Demonstrate proof of concept for each approach and prioritize by using decision flow charts

Gather info on pros and cons

Choose approach that has highest likelihood of success, is cheapest, easiest to integrate into current process flow.

Work with Endicott and E.Fishkill to guide process development

Wafer Level Underfill Decision Chart

Item	Choices	Status	Target date for decision	Lead person
Dispense Process	Spinning, Screening, Laminating	Spinning chosen		
Bumping	Bumps first or Bumps second	Tentatively Bumps 2nd		
Bumps	Pb-free solder or cond. adh.	In play		
Underfill	NS&C, other, reworkable, non-reworkable	In play		
Underfill post-dispense process	Laser ablation, Photoresist & etch, or photo-imageable	In play		
Underfill structural aspect	Single layer or bilayer	Patent disclosure pending		
Package topography	Planar or protruding bumps	In play		